AMENDMENTS TO THE CLAIMS

This listing of the claims will replace all prior versions and listings of the claims in this application.

Listing of the Claims:

1. (Currently amended) A method for organizing cache memory for hardware acceleration of the FDTD method in ~~a very high bandwidth,~~ dual-port on-chip memory, comprising:

creating a plurality of small banks of internal memory; and

~~arranging~~ routing data from the plurality of small banks of internal memory to computation engines so that all data dependencies of the computational engines are satisfied when each read address is presented to the plurality of small banks of internal memory~~capable of being statically wired~~.

2. (Currently amended) A method for organizing cache memory for hardware acceleration of ~~the~~ an FDTD method in ~~a very high bandwidth,~~ dual-port on-chip memory, comprising:

providing a first plurality of dual-port input memory banks that connect to corresponding one-cycle delay elements;

connecting the delay elements to corresponding computation engines;

providing a second plurality of input memory banks that connect to a second set of one-cyle delay elements;

connecting the second set of one-cyle delay elements to the corresponding computation engines;

and connecting the computation engines to corresponding output memory banks,

wherein said connecting steps route data dependent on direction from said memory banks to the corresponding computation engines when each read address is presented to said memory banks.

3. (Currently amended) A method for organizing cache memory as recited in claim 2,

wherein the first plurality of dual-port input memory banks handles fields having i and j directional dependencies.

4. (Currently amended) A method for organizing cache memory as recited in claim 3, wherein each of the first plurality of dual-port input memory banks includes a first ~~channel~~ port that handles fields having i directional dependencies, and a second ~~channel~~ port that handles fields having j directional dependencies.

5. (Original) A method for organizing cache memory as recited in claim 2, wherein the second plurality of input memory banks handles fields having k directional dependencies.

6. (Original) A method for organizing cache memory as recited in claim 2, wherein the output memory banks buffer updated fields before storing the updated fields to a bulk memory.

7. (Original) A method for organizing cache memory as recited in claim 2, wherein at least six output memory banks are provided.

8. (Currently amended) An organization scheme of cache memory for hardware acceleration of ~~the~~ an FDTD method in a ~~very high bandwidth,~~ dual-port on-chip memory, comprising:

a first plurality of input memory banks connected to corresponding one-cycle delay elements;

a plurality of computation engines connected to corresponding delay elements;

a second plurality of input memory banks connected to a second set of one-cycle delay elements;

connecting to the corresponding computation engines; and

a plurality of output memory banks and the second set of one-cyle delay elements connected to an output and an input, respectively, of the corresponding computation engines,

wherein said connecting steps route data, dependent on direction, from said memory banks to the corresponding computation engines when each read address is presented to said

memory banks.

9. (Original) An organization scheme of cache memory as recited in claim 8, wherein the first plurality of input memory banks handles fields having i and j directional dependencies.

10. (Original) An organization scheme of cache memory as recited in claim 9, wherein each of the first plurality of input memory banks includes a first channel that handles fields having i directional dependencies, and a second channel that handles fields having j directional dependencies.

11. (Original) An organization scheme of cache memory as recited in claim 8, wherein the second plurality of input memory banks handles fields having k directional dependencies.

12. (Original) An organization scheme of cache memory as recited in claim 8, wherein each of the plurality of output memory banks buffer update fields before storing the updated fields to a bulk memory.

13. (Original) An organization scheme of cache memory as recited in claim 8, wherein the plurality of output memory banks comprises at least six output memory banks.

14. (Currently amended) A method of using an organization scheme of cache memory for hardware acceleration of the an FDTD method in a very high bandwidth, dual-port on-chip memory, the organization scheme comprising:

~~a first plurality of input memory banks connected to corresponding one-cycle delay elements, a plurality of computation engines connected to corresponding delay elements, a second plurality of input memory banks connected to corresponding computation engines, and a plurality of output memory banks connected to corresponding computation engines, the method comprising:~~

loading dual fields of data into the first plurality of input memory banks, and simultaneously moving old values in the first plurality of input memory banks to the second plurality of input memory banks;

loading primary fields of data into the second plurality of input memory banks;

beginning computations and iterating over the primary fields of data with the plurality of computation engines;

storing updated fields in the plurality of output memory banks when updated fields emerge from plurality of computation engines; and

writing updated fields to bulk storage,

wherein the organization scheme further comprises a first plurality of dual-port input memory banks connected to corresponding one-cycle delay elements, a plurality of computation engines connected to corresponding delay elements, a second plurality of input memory banks connected to corresponding computation engines, and a plurality of output memory banks connected to corresponding computation engines.

15. (Original) A method of using an organization scheme of cache memory as recited in claim 14, wherein the loading dual fields for data into the first plurality of input memory banks continues until the first plurality of input memory banks are full.

16. (Original) A method of using an organization scheme of cache memory as recited in claim 14, further comprising: determining whether the method is complete, wherein if the method is complete, the method stops, otherwise the method moves to the next data and repeats.